CLAIMS

What is claimed is:

1. A method of forming an emitter in a vertical bipolar transistor comprising:

providing a substrate having a collector layer and a base layer over said collector layer;

forming a patterned mask over said collector layer; and

filling openings in said mask with emitter material in a damascene process.

2. The method in claim 1, wherein said substrate includes an insulator layer between a bottom silicon layer and a top silicon layer, said method further comprising:

implanting a first impurity to form said collector layer in a lower portion of said top silicon layer adjacent said insulator layer; and

implanting a second impurity to form said base layer in an upper portion of said top silicon layer.

3. The method in claim 2, wherein said emitter material includes said first impurity and said method further comprises annealing said vertical bipolar transistor to drive said first impurity into said base to create an emitter diffusion region in said base below each emitter.

4. The method in claim 2, further comprising:

patterning a second mask over said bipolar region, said mask including openings through to said base layer between adjacent ones of said emitters; and

implanting additional amounts of said second impurity into said base layer through said openings.

5. The method in claim 2, further comprising:

forming a protective layer over said emitters; and

implanting additional amounts of said first impurity into said insulator layer to provide a collector contact diffusion region.

6. A method of simultaneously forming complementary metal oxide semiconductor (CMOS) devices and vertical bipolar transistors on an integrated circuit chip comprising:

providing a silicon over insulator (SOI) substrate having a collector layer and a base layer over said collector;

forming a polysilicon layer over a CMOS region of said SOI substrate;

patterning a mask over said polysilicon layer and a bipolar region of said SOI substrate, said mask including openings over said bipolar region

depositing an emitter material in said openings in a damascene process to form emitters;

removing said mask;

patterning said polysilicon layer to form gate conductors; and

forming sidewall spacers adjacent said emitters and said gate conductors.

7. The method in claim 6, wherein said substrate includes an insulator layer between a bottom silicon layer and a top silicon layer, said method further comprising:

implanting a first impurity to form said collector layer in a lower portion of said top silicon layer adjacent said insulator layer; and

implanting a second impurity to form said base layer in an upper portion of said top silicon layer.

8. The method in claim 7, wherein said emitter material includes said first impurity and said method further comprises annealing said vertical bipolar transistor to drive said first impurity into said base to create an emitter diffusion region in said base below each emitter.

9. The method in claim 7, further comprising:

patterning a second mask over said bipolar region, said mask including second openings through to said base layer between adjacent ones of said emitters; and

implanting additional amounts of said second impurity into said base layer through said openings.

10. The method in claim 7, further comprising:

forming a protective layer over said emitters; and

implanting additional amounts of said first impurity into said insulator layer to provide a collector contact diffusion region.

11. The method in claim 6, further comprising, before said forming of said polysilicon, forming a gate oxide layer over said CMOS region of said SOI substrate.

12. A method of simultaneously forming complementary metal oxide semiconductor (CMOS) devices and vertical bipolar transistors on an integrated circuit chip comprising:

providing a silicon over insulator (SOI) substrate having a collector layer

and a base layer over said collector;

patterning a mask over a CMOS region and a bipolar region of said SOI substrate, said mask including first openings over said bipolar region;

depositing an emitter material in said first openings in a first damascene process to form emitters;

patterning said mask to form second openings over said CMOS region;

depositing a gate conductor material in said second opening in a second damascene process to form gate conductors;

removing said mask; and

forming sidewall spacers adjacent said emitters and said gate conductors.

13. The method in claim 12, wherein said substrate includes an insulator layer between a bottom silicon layer and a top silicon layer, said method further comprising:

implanting a first impurity to form said collector layer in a lower portion of said top silicon layer adjacent said insulator layer; and

implanting a second impurity to form said base layer in an upper portion of said top silicon layer.

14. The method in claim 13, wherein said emitter material includes said first impurity and said method further comprises annealing said vertical bipolar transistor to drive said first impurity into said base to create an emitter diffusion region in said base below each emitter.

15. The method in claim 13, further comprising:

patterning a second mask over said bipolar region, said mask including third openings through to said base layer between adjacent ones of said emitters; and

implanting additional amounts of said second impurity into said base layer through said third openings.

16. The method in claim 13, further comprising:

forming a protective layer over said emitters; and

implanting additional amounts of said first impurity into said insulator layer to provide a collector contact diffusion region.

17. The method in claim 12, further comprising, before said forming of said polysilicon, forming a gate oxide layer over said CMOS region of said SOI substrate.

18. A semiconductor structure including both a CMOS transistor and a vertical bipolar transistor, comprising:

a substrate having a lower semiconductor portion, an upper semiconductor portion, and an first insulator structure between said upper and lower semiconductor portions;

a collector region disposed in the upper semiconductor portion, said collector region having a peak dopant concentration adjacent the first insulator structure;

a plurality of base regions disposed in the upper semiconductor portion above the collector region;

a plurality of emitter diffusion regions disposed in the upper semiconductor portion, each abutting a respective one of the plurality of base regions;

a second insulator structure disposed on first selected portions of the upper semiconductor portion;

a plurality of first electrodes disposed on the upper semiconductor portion, each of the plurality of first electrodes forming an electrical contact to a respective one of the plurality of emitter diffusion regions; and

a second electrode formed on the second insulator structure, the second electrode comprising a gate electrode of the CMOS transistor.

19. The structure in claim 18, wherein the plurality of base regions and the plurality of emitter diffusion regions are surrounded by the collector region.

20. The structure in claim 19, further comprising a plurality of oxide isolation regions that abut the collector region.

21. The structure in Claim 18, wherein both of said plurality of first electrodes and said second electrode are comprised of a common polysilicon layer.

22. The structure of Claim 19, wherein the collector region extends substantially to an upper surface of the upper semiconductor portion.